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| **PES University Logo.jpg** | **PES University, Bangalore**  (Established under Karnataka Act No. 16 of 2013) | UE18CS253 |
| **Model Question Paper B.TECH. IV SEMESTER**  **UE18CS253- Microprocessors & Computer Architecture** | | |
| Time: 3 Hrs Answer All Questions Max Marks: 100 | | |

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| 1. | a) | Differentiate the following   1. Microprocessors and Microcontroller. 2. Computer Organization and Computer Architecture. 3. RISC and CISC. | 06 |
| b) | Write a program using ARM ISA to find the length of a string. | 03 |
| **c)** | The address for the memory system starts from 1000. It is byte addressable and follows little endian. Show the memory allocated for the following data declaration in ARM memory organization.  a:.halfword 400  b:.byte 40,80,90  c:.halfword 50  d:.halfword 10  e:.word 600 | 05 |
| **d)** | Write the equivalent ARM code snippet for the following C–language statement.  I)  int fun (int I, int j)  {  while (i!=j)  {  if (i>j)  i -= j;  else  j -= i;  }  }  **2)**  While( i < 5 )  { x[i] = y + i;  i + = 1;  } | 06 |
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| 2 | a) | Explain pipelining with an example. | 03 |
| b) | Consider two instructions *i* and *j*, with *i* occurring before *j*. Explain the possible data hazards. | 06 |
| c) | How data hazards are minimized using data forwarding in a 5 stage pipeline architecture? Explain with a neat diagram. | 04 |
| d) | Consider the following RISC assembly code.    load r1,45(r2) (1)  add r7 <- r1, r5 (2)  sub r8 <- r1, r6 (3)  or r9 <- r5, r1 (4)  brneq r7, target (5)  add r10 <- r8, r5 (6)  xor r2 <- r3, r4 (7)  Identify each dependence; list the two instructions involved; identify which instruction is dependent; and, if there is one, name the storage location involved (register or memory). | 07 |
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| 3. | a) | A computer has an 8 GByte memory with 64 bit word sizes. Each block of memory stores 16 words. The computer has a direct-mapped cache of 128 blocks. The computer uses word level addressing. What is the address format? If we change the cache to a 4- way set associative cache, what is the new address format? | 08  (4+4) |
| b) | Find the average memory access time for a processor given the following:  - The clock rate is 1 ns  - The miss penalty is 25 clock cycles  - 1% of instructions are not found in the cache.  - 5% of data references are not found in the cache  - 15% of memory accesses are for data.  - The memory system has a cache access time (including hit detection) of 1 clock cycle.  - Assume that the read and write miss penalties are the same and ignore other write stalls. | 4 |
| c) | Briefly explain the different write strategies. | 06 |
| d) | What is principle of locality of reference ? | 02 |
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| 4. | a) | “Multi level cache reduces miss penalty”. Justify the statement with an example. | 05 |
| b) | Write a note on DMA. | 05 |
| c) | Write a note on Flynn’s Classification of parallel computing. And Explain any one classification with an example. | 06 |
| d) | Explain the following techniques   1. Polling 2. Daisy Chain Technique | 04 |
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| 5. | a) | Write the limitations of serial computing and the applications of parallel computing. | 05 |
| b) | What is instruction level parallelism?Consider the following program:  e = a + b  f = c + d  m = e \* f  If we assume that each operation can be completed in one unit of time what is the total amount of time required to execute the above program? | 05 |
| c) | What is Cache Coherency? Explain with an example. | 05 |
| d) | Mention the limitations of ILP | 05 |